IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Hiroshi Mizuhashi — Group Art Unit: 2827

Serial No.: 10/806,350 — Examiner: T. Phan

Filed: March 23, 2004 — Confirm. No.: 3991

For: METHOD OF TRANSFERRING DATA

AMENDMENT UNDER 37 C.F.R. 1.116

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11/22/07

Date: November 6, 2007

Sir:

In response to the Final Office Action dated June 6, 2007, the period for response having been extended two (2) months to November 6, 2007, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

An output signal of the NOR circuit 22 is also used for the equalizing signal EQS to drive the equalizing circuit 304. A NOR circuit 51 providing signal TGL and an inverter 52 providing signal TGLb drive the transfer gate 302 by the VDD level in response to the equalizing signal EQLb and the block selecting signal YBSEL. A NOR circuit 53 providing signal TGR and an inverter 54 providing signal TGRb drive the transfer gate 303 by the VDD level in response to the equalizing signal EQRb and the block selecting signal YBSEL.

In this embodiment, the P-channel transistor 55 and the N-channel transistor 214 are connected in parallel between the sense amplifier 301 and the left bit line BL. Therefore, even if the transistors 55 and 214 are driven by the voltage VDD, the data can be transferred without a voltage drop. When the input node SBL is the "H" level, the ~~N~~ P-channel transistor 55 which is driven by the VDD level generates the voltage drop Vt caused by the threshold voltage. At the P-channel transistor 214 which is driven by the GND level, the voltage drop caused by the threshold voltage ~~dose~~ does not occur when the input node SBL is the "H" level. As a result, the "H" level of the input node SBL in the sense amplifier 301 can be transferred to the bit line BL without the voltage drop. When the input node SBL is the "L" level, the ~~P~~ N-channel transistor 214 generates the voltage drop caused by the threshold voltage. However, the ~~N~~ P-channel transistor 55 does not generate the voltage drop when the bit line voltage is the "L" level. As a result, the "L" level of the input node SBL in the sense amplifier 301 can be transferred to the bit line BL without the voltage drop.

Inverters 21 and 23 are driven by the Vpp level, and drive the pre-charge circuits 305 and 306 by producing signals EQL and EQR respectively in response to the